IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Newell Chiesl

Serial No. :	09/960,441	**Group Art Unit :**	2812
Filed :	September 21, 2001	**Examiner :**	Simkovic, V.
For :	Arrangement For Measuring Pressure on a Semiconductor Wafer and an Associated Method For Fabricating a Semiconductor Wafer	**Atty Docket :**	1003-0610 / 01-384

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

April 13, 2004 — Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 13 APR 04